(b) Discuss the various possible hazards between read and write operations in an instruction pipeline and state the mechanism to detect and avoid these hazards. Also discuss the dynamic instruction scheduling.

(c) Consider the execution of a program of 15,000 instructions by a linear pipeline processor with a clock rate of 25 MHz. Assume that the instruction pipeline has five stages and that one instruction and out-of-sequence executions are ignored.

(i) Calculate the speedup factor in using this pipeline to execute the program as compared with the use of an equivalent nonpipelined processor with an equal amount of flow-through delay.

(ii) What are the efficiency and through put of this pipelined processor?



PAPER ID : 1067

**TCS-401/TIT-401** **Printed Pages : 4**

Paper ID and Roll No. to be filled in your Answer Book

Roll No. 1 0 7 2 0 1 0 2 0 9

# B.Tech.

(SEM. IV) EXAMINATION, 2012

## COMPUTER ORGANIZATION

Time : 3 Hours] [Total Marks : 100

**Note :** Attempt all questions. All question carry equal marks.

1 Attempt any Four parts of the following: 5×4=20

(a) What do you mean by inter-register transfer? Discuss Bus transfer.

(b) Design Arithmetic Logic Shift unit that will perform different arithmetic, logic an shift operation..

(c) Draw a diagram of bus system for four registers of 4-bits each. The bus is to be constructed with multiplexers.

(d) Show the hardware implementation for the following statements. The registers are 4-bits in lengths :

TO : A ← RQ

TI : A ← R1

T2 : A ← R2

T3 : A ← R3

(e) Show the multiplication process using Booth's algorithm when the following binary numbers are multiplied: (12)*(-18)



2784 25

(f) Represent the decimal number -0.654 into IEEE floating point format.

2 Attempt any Four parts of the following : **10×2=20**

(a) Explain the Fetch and Execute cycle during execution of an instruction.

(b) Describe briefly a Hardwired Control.

(c) What is microinstruction? Describe the microinstruction format.

(d) What do you mean by the term Microprogram Sequence' Explain the role played by it.

(e) Discuss advantages and disadvantages of Microprogrammed Control

(f) Explain wide-branch addressing and emulation.

3 Attempt any Two parts of the following : **10×2=20**

(a) Write a program to evaluate the arithmetic expression: X=(A+B*C)/(D+E*F/G+H) Using Three, Two, One and Zero address Instructions.

(b) Design an efficient logic circuit shared by different branch conditions derived from the combination or stand alone status of the Flag register bits S (sign), V (overflow), C (End carry), Z (all O's). Specify the conditional branch instructions which can be supported by the circuit you have designed.

(c) Describe DMA with suitable block diagram. Why does DMA have priority over the CPU when both request a memory transfer? Explain,



4 Attempt any Two parts of the following : **10x2=20**

(a) The access time of a cache memory is 100 ns and that of main memory 1000 ns. It is estimated that 80 percent, of the memory requests are for read and the remaining' 20 percent for write. The hit ratio for read accesses only is 0.9.

(i) What is the average access time of the system considering only memory read cycles?

(ii) What is the average access time of the system for both read and write requests?

(iii) What is the hit ratio taking into consideration the write cycles?

(b) A block set associative cache consists of a total of 64 blocks divided into four block sets. The main memory containing 4096 blocks each consisting of 128 words.

(i) How many bits are there in the main memory address?

(ii) How many bits are there in each of TAG, SET and WORD field?

(c) Discuss the concept and implementation of virtual memory. Also describe a suitable scheme for translation from logical address to physical address.

5 Attempt any Two parts of the following : **10×2=20**

(a) Give various architectural classification schemes. Also discuss the Flynn's and Feng's classification in detail.