diagram of a 4-bit register with using D flip-flop.

Note: Attempt all questions. Be precise in your answer.

SECTION A

Q1:- Attempt any **four** of the following : **4×5=20**

1. Derive a circuit that implement the Boolean function Y = (AB + CD + AED + CEB)' using six MOS transistors.
2. Convert the following numbers with the indicated bases to decimal :
   (a) $(198)_{12}$
   (b) $(735)_8$
   (c) $(16.5)_{16}$
3. Draw the circuit diagram of 3-input TTL NAND gate with totem pole output and discuss its operation.

SECTION B

Q2:- Attempt any **four** of the following : **4×5=20**

1. Implement a full adder with a decoder and NAND gates.
2. Design an excess 3 to BCD decoder using the unused combinations of the code as don't care conditions
3. Design a 2-bit comparator using logic gates.
4. Implement a 16:1 Multiplexer using 4:1 Multiplexers.
5. Design a 2-bit comparator using logic gates.
6. Implement the fuction
   Y = A'B'C + ABCD' + A'BCD + AB + C using **PLA**.

SECTION C

Q3:- Attempt any **two** of the following : **10×2=20**

1. What is race-around condition? How does it get eliminated in master-slave J-K flip-flop?
2. Design and implement a MOD-8 synchronous up/down counter using J-K flip-flop?
3. Explain how to convert serial data. What type of register is needed? Design the logic

SECTION D

Q4:- Attempt any **two** of the following : **10×2=20**

1. Derive a circuit that implement the Boolean function Y = (AB + CD + AED + CEB)' using six MOS transistors.
2. **(a)** Using the NOR output of two ECL GATE, show that, when connected together to an external resistor and a negative supply voltage, the wired connection produces an OR function.
   (b) Calculate the noise margin of the ECL gate.
3. Draw the circuit diagram of 3-input TTL NAND gate with totem pole output and discuss its operation.

SECTION E

Q5:- Attempt any **two** of the following : **10×2=20**

1. What are the different types of hazards in asynchronous sequential circuits? Differentiate static-0 and static-1 hazards with waveform.
2. How does a static RAM cell differ from a dynamic RAM cell? What timing parameters determine its operating speed? Draw the typical write cycle timing for static RAM.
3. **(a)** Write a short note on one and multidimensional selection arrangement of memories.
   (b) Design a combinational circuit using ROM. The circuit accepts 3-bit number and output a binary number equal to the square of the input number.