

2. Analyze the circuit shown in fig. 1 to produce Boolean algebraic expression for the circuit outputs.

1. Determine the base b in each of the following cases:

(a) $(361)_{10} = (551)_b$

(b) $(859)_{10} = (5E7)_b$

2. Write the 8-bit signed magnitude, 2's complement and 1's complement from the following decimal numbers:

(a) +119

(b) -77

3. Write out the first ten numbers for a decimal weighted codes: 7421, 2421, 2401, 8421, 5421, 5021, 5201, 5210, 5010, 5011

4. Using the theorems of Boolean algebra simplify the following expression:

$$F(A, B, C, D) = B + BCD + \bar{B}CD + AB + \bar{A}B + \bar{B}C$$

5. What is difference between a Latch and a flip-flop?

6. What is race around condition and how it is overcome?

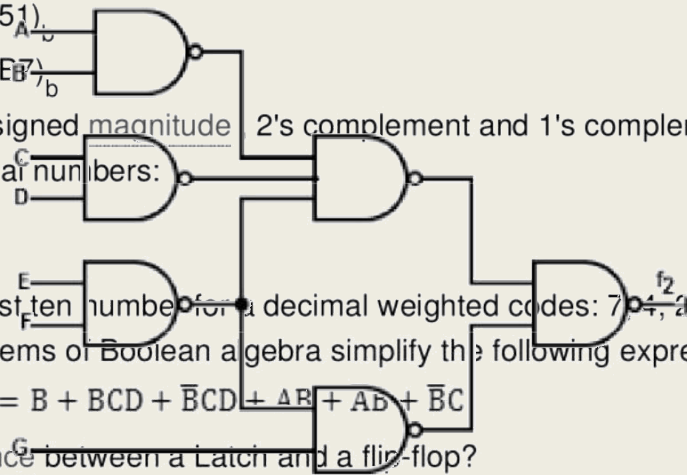


Fig. 1

Attempt any two parts of the following:

1. Construct a truth table for the following functions and from the truth table obtain an expression for the inverse function using only NOR gates having a maximum fan-in of three:

(i) $F(A, B, C) = A + B\bar{C}$
 $f = (\bar{A} + B)(\bar{C} + D)(B + C)(\bar{A} + D)(\bar{A} + C)$
 (ii) $F(A, B, C) = (A + B)(A + B + C)$

2. For the following two 4-variable functions

empt any two parts of the following:

$$f_1 = A + B + C + D$$

1. Implement the following 3-variable Boolean function using 4-input multiplexers:

$$f = \sum(0, 2, 3, 5, 7)$$

2. Design a circuit for converting from the 8421 code to the 5421 code and implement the design with 4-to-1 multiplexers. What are the minterms expressions for the two functions? Simplify both functions using the theorems of Boolean algebra.

3. Develop a 3-to-8 line decoder using NOR gates only, and draw its logic diagram.

3. Simplify the following three-variable Boolean function algebraically and express them in terms of product of maxterms:

empt any four parts of the following:

(a) $f_1 = \sum(1, 2, 5, 6)$

(b) $f_2 = \sum(0, 1, 2, 3, 7)$

1. Differentiate between the working of static and dynamic memory. Also discuss the difference between SRAM and DRAM.

Design a synchronous modulo-12 counter using NAND gates and T flip-flops.

3. Design a hazard free, D-type flip-flop using asynchronous circuit design techniques. It may be assumed that the output will take on the value of the input on the trailing edge of a clock pulse.

$$f = \sum(0, 2, 8, 9, 10, 12, 13, 14)$$