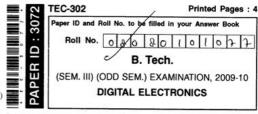
5	Attempt	anv	two	out	of	three

2×10

- (a) Explain with the help of circuit diagram the operation of ECL OR/NOR gate. Show that the transistors in the circuit operate in the active region and not in saturation. Calculate the noise margin (Assume V_{BE, active} = 0.7 V)
- (b) If CMOS and TTL gates are used in the same circuit what current and voltage conditions must be satisfied when
 - (i) CMOS gate is driving TTL gates
 - (ii) TTL gate is driving CMOS gates
- (c) Explain the working of TTL NAND gate. What is totem-pole output and open-collector output. Which configuration can be used for wired-AND ?



Time ; 3 Hours]

[Total Marks: 100

Note: Attempt all questions.

Attempt any four parts of the following :

5×4=20

- What are the characteristics of Gray code ? Design a circuit for converting (i) a 4-bit binary number into Gray code (ii) 4-bit Gray code into corresponding straight binary number.
- (b) Explain the following characteristics of digital IC's :
 - (i) Propagation delay
 - (ii) Figure of merit
 - (iii) Noise margin
 - (iv) Voltage parameters
- 'A' transmits Hamming code (Even parity) for a BCD digit and 'B' receives 0110000. Assuming that only one-bit can be in error during the transmission, find out the BCD digit that was transmitted by A.

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[3420]

[Contd...

- (d) Explain the concept of Duality in Boolean algebra.
- (e) Design a full adder circuit using a 3-to-8 decoder with active low outputs and minimum number of gates.
- (f) Explain the operation of CMOS NAND gate.
- 2 Attempt any four parts in this question: 5×4=2
 - (a) Explain the concept of Implicant, Prime implicant and essential prime implicant taking a suitable example.
 - (b) Design a 5-to-32 line decoder using 3-to-8 line decoder.
 - (c) Implement the following Boolean function using single 8 × 1 multiplexer.

$$f(A, B, C, D) = \sum m(1, 2, 5, 6, 9, 11, 12, 15)$$

- (d) What are static and dynamic hazards? How do you eliminate these hazards?
- (e) Draw the structure of a static RAM cell and explain its working.
- (f) Design a one-digit BCD subtractor.

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3 Attempt any two parts of the following :

2×10

(a) Given the function

$$f(A, B, C, D) = \sum m(0, 4, 9, 10, 11, 12)$$
 and $f_1 = B \oplus D$. Determine f_2 and f_3 such that $f = f_1 f_2 + \overline{f_3}$.

(b) Realize the following multiple output function using 3 × 4 × 2 PLA:

$$f_1(x, y, z) = \sum m(0, 1, 3, 5)$$

 $f_2(x, y, z) = \sum m(3, 5, 7)$

- (c) Design a 4-stage carry look ahead adder.
- 4 Attempt any two out of three :

npt any **two** out of three : 2×10

Design a register (4-bit) using multiplexers and

D-flipflops having the behaviour specified below:

Selec	t line	
S_1	S_0	Register operation
0	0	Hold
0	1	Synchronous clear
1	0	Complement contents
1	1	Circular shift right

- (b) Write the excitation table for J-K FF and T-FF. Convert a D-FF into J-K flip-flop.
- (c) Design a 4-bit synchronous UP/DOWN counter.

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2

[Contd...