B. TECH. IInd - Year

THIRD SEMESTER EXAMINATION, 2007-2008

TCS-301 COMPUTER ORGANIZATION

Time : 3 Hours *Maximum Marks : 100*

Note : Attempt any *FIVE* questions.

1. (*a*) Draw a diagram of a bus system for four resistors that uses three state buffer and a decoder instead of multiplexers. **(6)**

(*b*) Show the multiplication process using Booth's algorithm, when the following binary numbers are multiplied :

(-11)*(-14) **(7)**

(*c*) Explain the biased exponent floating point representation. **(7)**

2. (*a*) Define the following :

(*i*) Micro-operation

(*ii*) Micro-instruction

(*iii*) Direct addressing **(6)**

(*b*) What is the difference between RISC and CISC machines ? Write the RISC instructions in assembly language that will cause a jump to address 3200 if Z (zero) status bit is equal to one using immediate mode. **(7)**

(*c*) Discuss why interfacing is used in digital computers. Explain salient features of a device interface. **(7)**

3. (*a*) Perform the following conversions :

(*i*) $(623.77)_{10} = (\quad)_2$

(*ii*) $(11010111.110)_2 = (\quad)_8$

(*iii*) $(204.1250)_{10} = (\quad)_{16}$

(*iv*) $(3A.2F)_{16} = (\quad)_{10}$ **(6)**

(*b*) A digital function is specified as $f(A,B,C) = \Sigma(1,2,4,5)$. Give its minimized NAND gate implementation. **(7)**

(*c*) Write an assembly program to evaluate the arithmetic statement $X = (A + B * C)/(D - E * F + G * H)$ using general resister type computer with three address instructions. **(7)**

4. (*a*) What is the purpose of counters ? How is the Ripple counter different to that of synchronous counter? Draw a logic diagram of 2 bit synchronous counter. **(10)**

(*b*) Design a counter which counts as follows –

000 – 001 – 010 – 011 – 100 – 101. The sequence repeats. **(10)**

5. (*a*) Describe Vector Processor and Array Processor. Explain their similarities and difference. **(10)**

(*b*) Give a brief description of the various I/O bus architectures. **(10)**

6. (*a*) How do CPU and DMA controllers work when they share single set of buses ? Explain it with the help of cycle stealing diagram. **(10)**

(*b*) Explain various cache mapping techniques. A computer system has a 4K word cache organized in block set associative manner with 4 blocks per set, 64 words per block. The main memory contains 65536 blocks. How many bits are there in each of the TAG, SET and WORD fields ? **(10)**

7. (*a*) Discuss the various organizations of RAM. A computer uses RAM chips of 1024x1 capacity. How many chips are needed and how should their address lines be connected to provide a memory capacity of 2048 bytes ? **(10)**

(*b*) Design MOD-12 Counter by using T-flip flops. **(10)**

